CS 33

Machine Programming (2)

CS33 Intro to Computer Systems

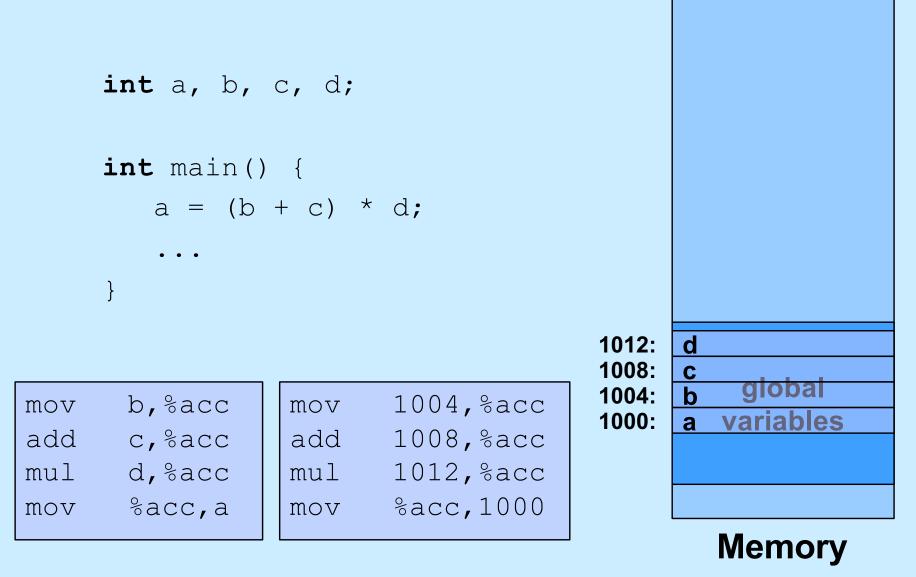
X–1

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Jump Instructions

- Unconditional jump
 - just do it
- Conditional jump
 - to jump or not to jump determined by conditioncode flags
 - field in the op code indicates how this is computed
 - in assembler language, simply say
 - » je
 - jump on equal
 - » jne
 - jump on not equal
 - » jg
 - jump on greater than (signed)
 - » etc.

Addresses



Addresses

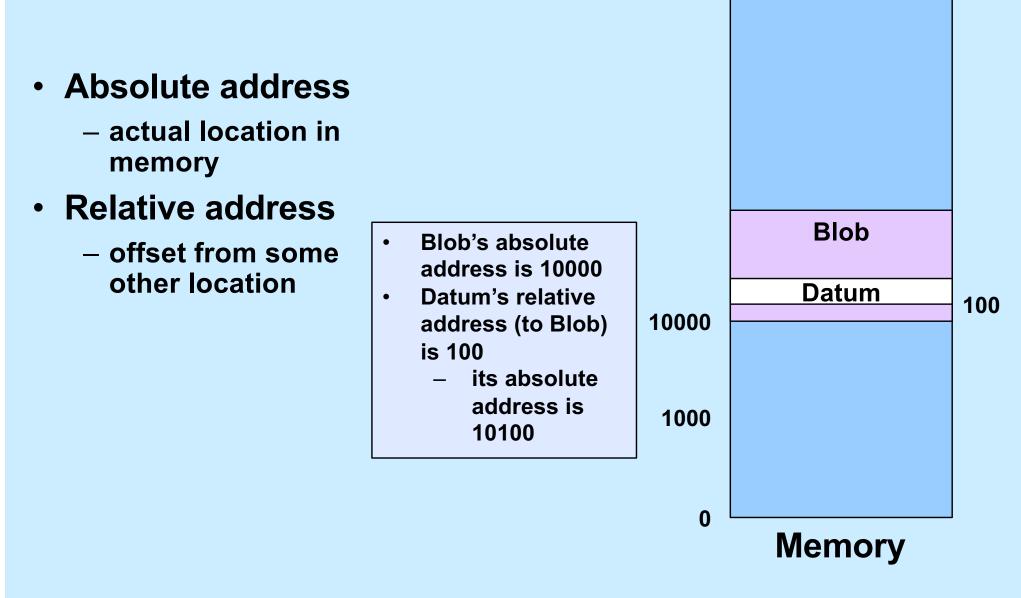
int b;

```
int func(int c, int d) {
   int a;
   a = (b + c) * d;
                            One copy of b for duration of
                         •
                            program's execution
                             • b's address is the same in
                                each call to func
   mov ?, %acc
                            Different copies of a, c, and d
   add ?, %acc
                            in each call to func

    addresses are different in

   mul ?, %acc
                                each call
           %acc,?
   mov
```

Relative Addresses

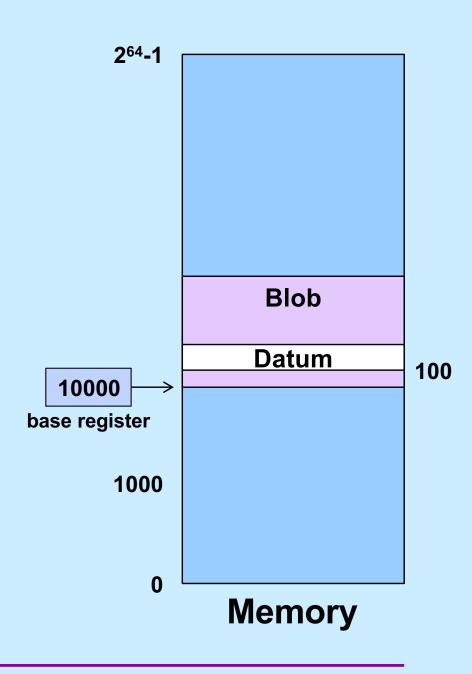


X-5

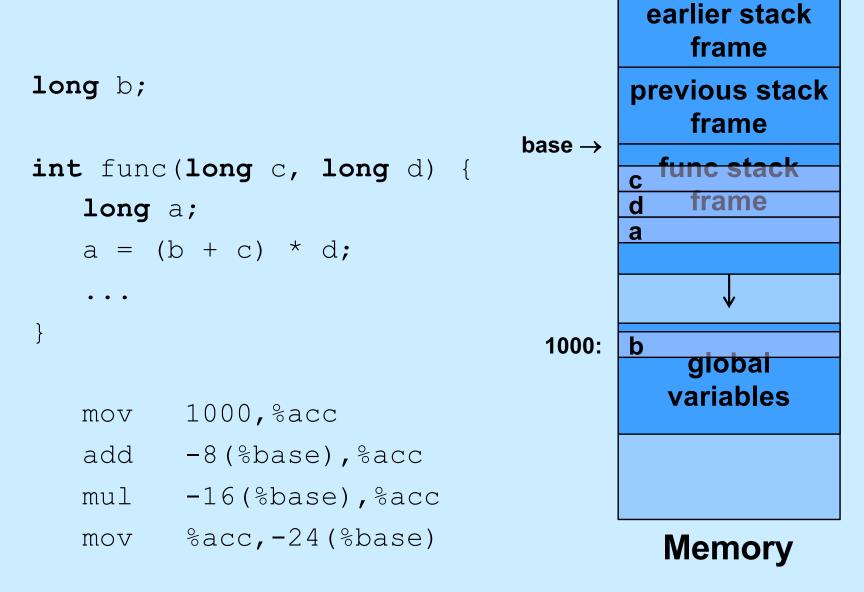
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Base Registers

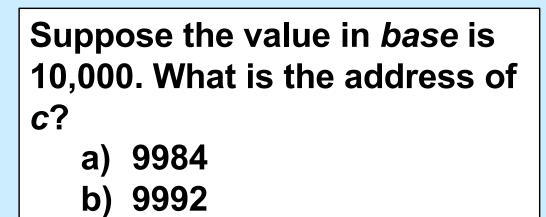
mov \$10000, %base
mov \$10, 100(%base)

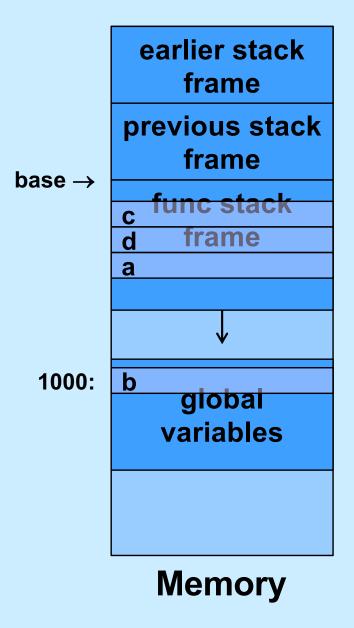


Addresses



Quiz 1





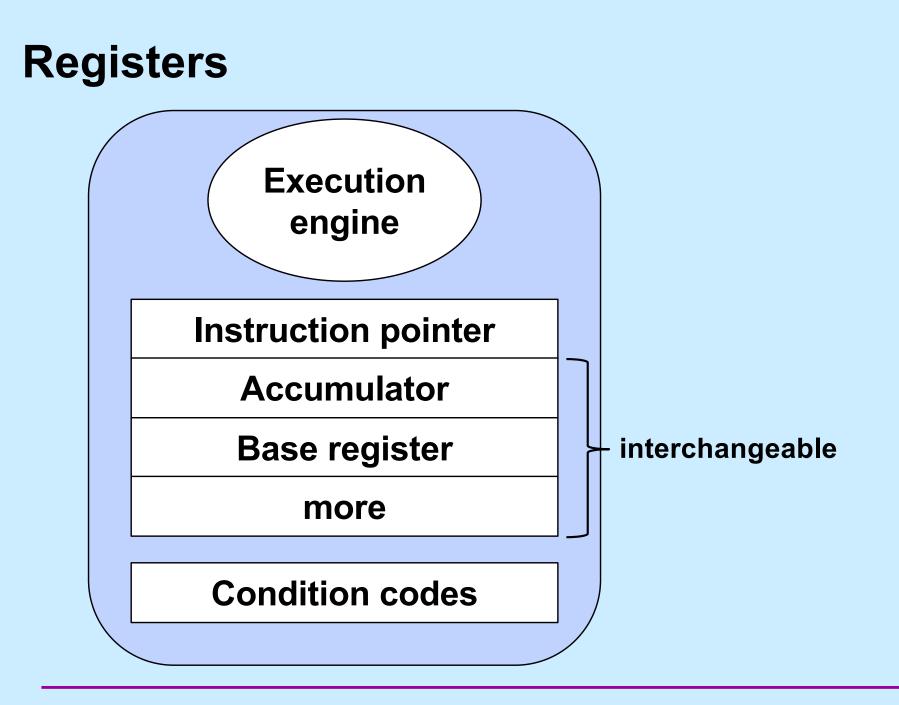
mov 1000,%acc

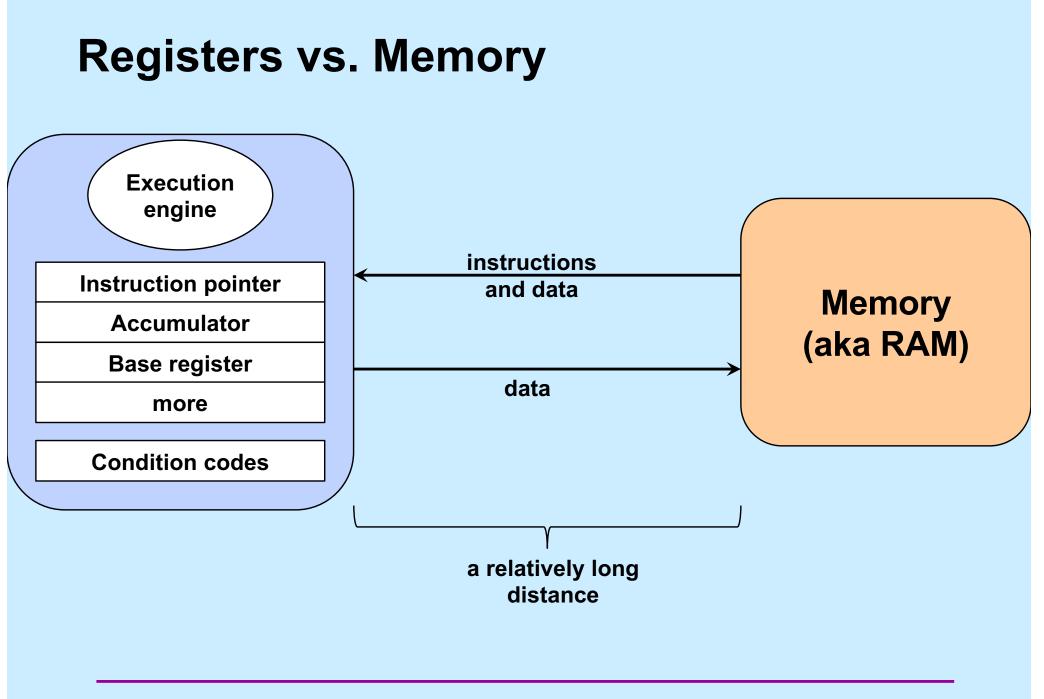
- add -8(%base),%acc
- mul -16(%base),%acc
- mov %acc,-24(%base)

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c) 10,008

d) 10,016





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Intel x86

- Intel created the 8008 (in 1972)
- 8008 begat 8080
- 8080 begat 8086
- 8086 begat 8088
- 8088 begat 286
- 286 begat 386
- 386 begat 486
- 486 begat Pentium
- Pentium begat Pentium Pro
- Pentium Pro begat Pentium II
- ad infinitum

IA32

2⁶⁴

• 2³² used to be considered a large number

one couldn't afford 2³² bytes of memory, so no problem with that as an upper bound

Intel (and others) saw need for machines with 64-bit addresses

- devised IA64 architecture with HP
 - » became known as Itanium
 - » very different from x86
- AMD also saw such a need
 - developed 64-bit extension to x86, called x86-64
- Itanium flopped
- x86-64 dominated
- Intel, reluctantly, adopted x86-64

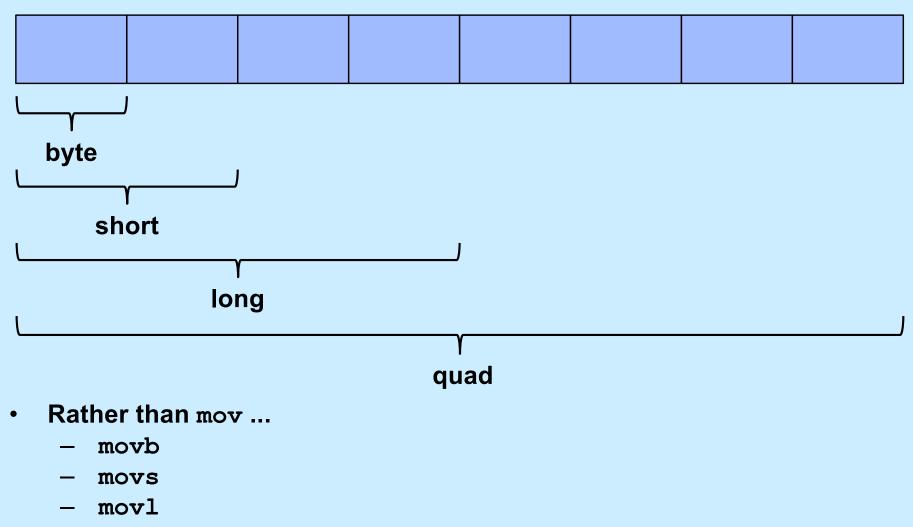
Why Intel?

- Most CS Department machines are Intel
- An increasing number of personal machines are not
 - Apple has switched to ARM
 - packaged into their M1, M2, etc. chips
 - » "Apple Silicon"
- Intel x86-64 is very different from ARM64 internally
- Programming concepts are similar
- We cover Intel; most of the concepts apply to ARM

Data Types on IA32 and x86-64

- "Integer" data of 1, 2, or 4 bytes (plus 8 bytes on x86-64)
 - data values
 - » whether signed or unsigned depends on interpretation
 - addresses (untyped pointers)
- Floating-point data of 4, 8, or 10 bytes
- No aggregate types such as arrays or structures
 just contiguously allocated bytes in memory

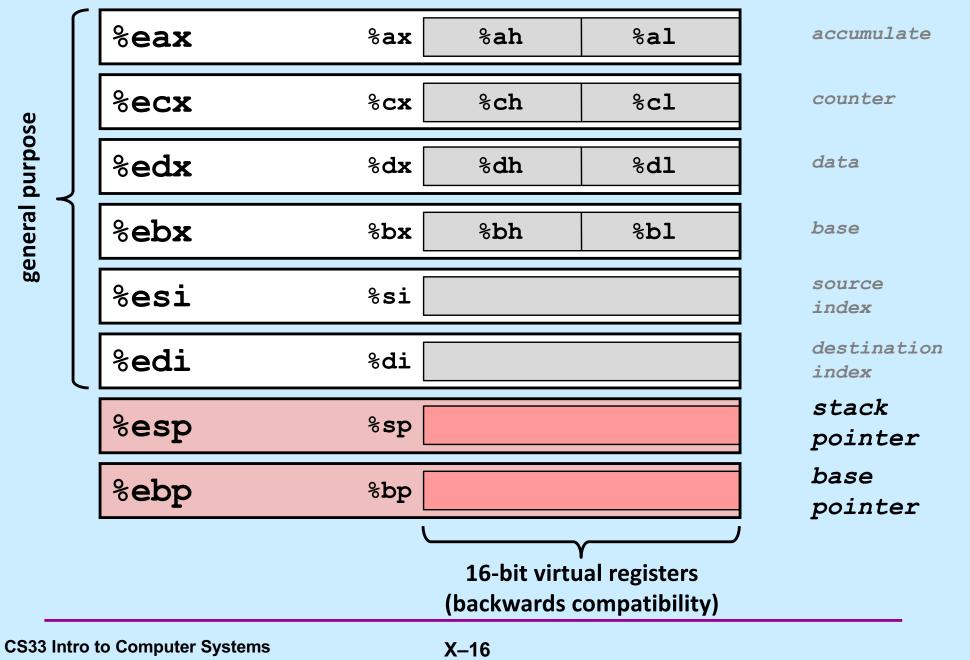
Operand Size



- movq (x86-64 only)

General-Purpose Registers (IA32)

Origin (mostly obsolete)



x86-64 General-Purpose Registers

%rax	%eax		8 r8	%r8d	a5
%rbx	%ebx		8 r9	%r9d	a6
%rcx	%ecx		% r10	%r10d	
%rdx	%edx		% r11	%r11d	
%rsi	%esi		% r12	%r12d	
%rdi	%edi		% r13	%r13d	
%rsp	% esp		% r14	% r14d	
%rbp	%ebp		%r15	% r15d	
	%rbx %rcx %rdx %rsi %rdi %rsp	%rbx %ebx %rcx %ecx %rdx %edx %rsi %esi %rdi %edi %rsp %esp	%rbx%ebx%rcx%ecx%rdx%edx%rsi%esi%rdi%esi%rdi%edi	%rbx%ebx%r9%rcx%ecx%r10%rdx%edx%r11%rsi%esi%r12%rdi%edi%r13%rsp%esp%r14	%rbx%ebx%r9%r9d%rcx%ecx%r10%r10d%rdx%edx%r11%r11d%rsi%esi%r12%r12d%rdi%edi%r13%r13d%rsp%esp%r14%r14d

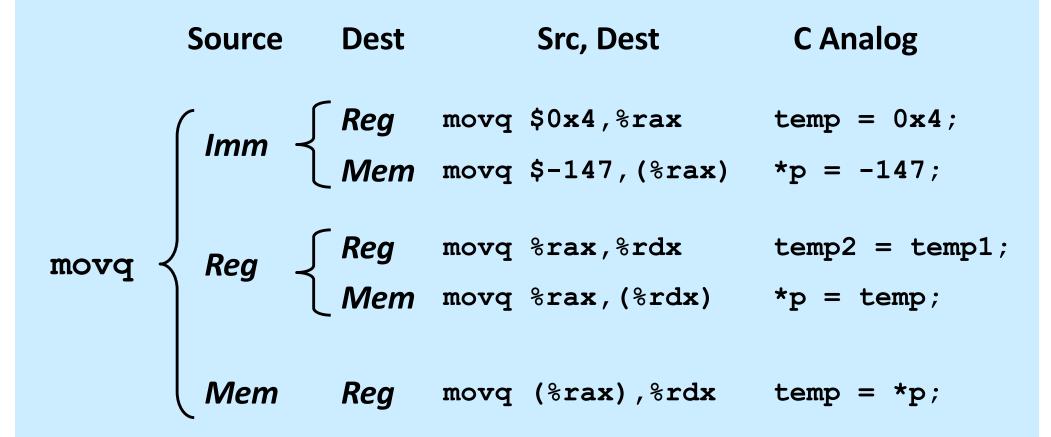
- Extend existing registers to 64 bits. Add 8 new ones.

Moving Data

- Moving data movq source, dest
- Operand types
 - Immediate: constant integer data
 - » example: \$0x400, \$-533
 - » like C constant, but prefixed with `\$'
 - » encoded with 1, 2, 4, or 8 bytes
 - Register: one of 16 64-bit registers
 - » example: %rax, %rdx
 - » %rsp and %rbp have some special uses
 - » others have special uses for particular instructions
 - Memory: 8 consecutive bytes of memory at address given by register(s)
 - » simplest example: (%rax)
 - » various other "address modes"



movq Operand Combinations



Cannot (normally) do memory-memory transfer with a single instruction

Simple Memory Addressing Modes

Normal (R) Mem[Reg[R]]
 – register R specifies memory address

movq (%rcx),%rax

Displacement D(R) Mem[Reg[R]+D]

 register R specifies start of memory region
 constant displacement D specifies offset

movq 8(%rbp),%rdx

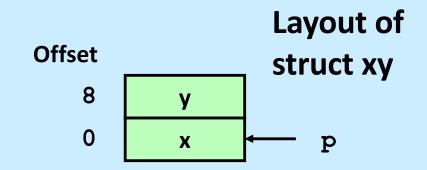
Using Simple Addressing Modes

```
struct xy {
    long x;
    long y;
}
void swapxy(struct xy *p) {
    long temp = p->x;
    p->x = p->y;
    p->y = temp;
}
```

```
swap:
```

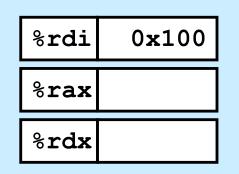
```
movq (%rdi), %rax
movq 8(%rdi), %rax
movq 8(%rdi), %rdx
movq %rdx, (%rdi)
movq %rax, 8(%rdi)
ret
```

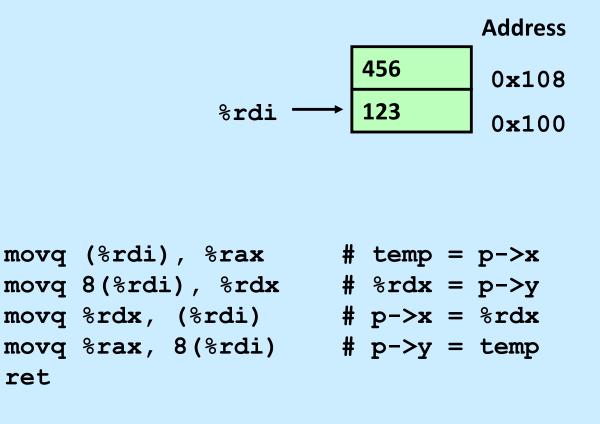
```
struct xy {
    long x;
    long y;
}
void swapxy(struct xy *p) {
    long temp = p->x;
    p->x = p->y;
    p->y = temp;
}
```



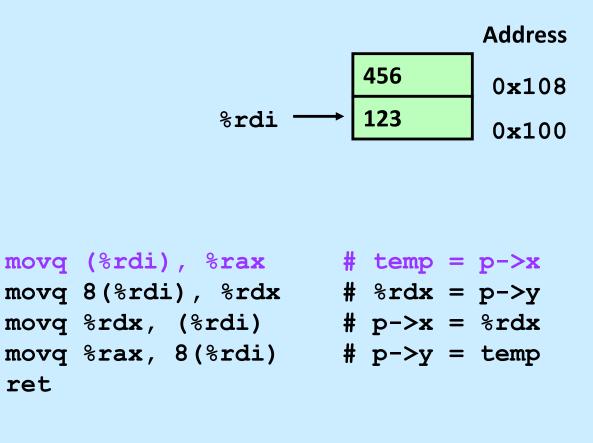
Register	Value
%rdi	Р
%rax	temp
%rdx	p->y

movq	(%rdi), %rax
movq	8(%rdi), %rdx
movq	%rdx, (%rdi)
movq	%rax, 8(%rdi)
ret	

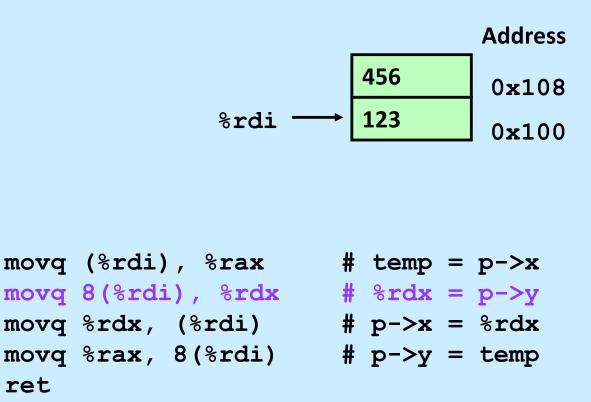




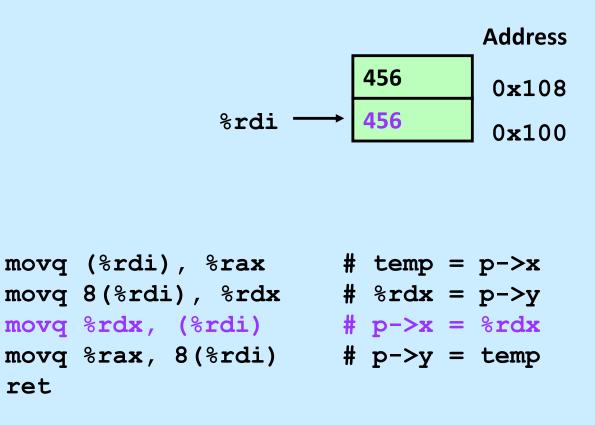
%rdi	0x100
%rax	123
%rdx	



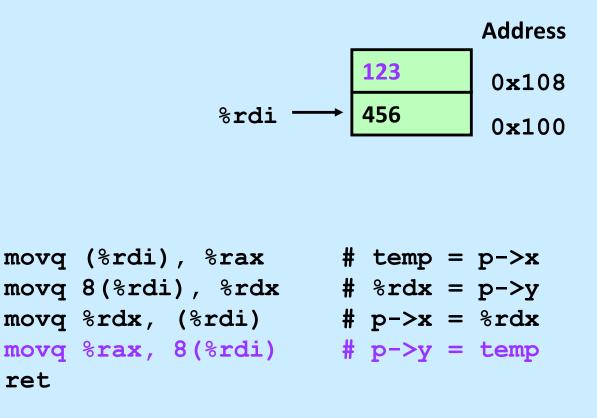
%rdi	0x100
%rax	123
%rdx	456



%rdi	0x100
%rax	123
%rdx	456

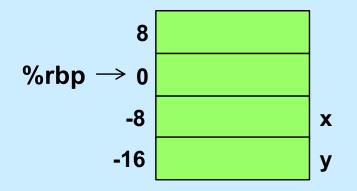


%rdi	0x100
%rax	123
%rdx	456



Quiz 2

movq -8(%rbp), %rax
movq (%rax), %rax
movq (%rax), %rax
movq %rax, -16(%rbp)



Which C statements best describe the assembler code?

// a	// b	// c	// d
<pre>long ***x;</pre>	<pre>long **x;</pre>	<pre>long *x;</pre>	<pre>long x;</pre>
long y;	long y;	long y;	long y;
y = ***x;	y = * * x;	y = *x;	y = x;

Complete Memory-Addressing Modes

Most general form

D(Rb,Ri,S) Mem[Reg[Rb]+S*Reg[Ri]+D]

- D: constant "displacement"
- Rb: base register: any of 16[†] registers
- Ri: index register: any, except for %rsp
- S: scale: 1, 2, 4, or 8
- Special cases

(Rb,Ri)	Mem[Reg[Rb]+Reg[Ri]]
D(Rb,Ri)	Mem[Reg[Rb]+Reg[Ri]+D]
(Rb,Ri,S)	Mem[Reg[Rb]+S*Reg[Ri]]
D	Mem[D]

[†]The instruction pointer may also be used (for a total of 17 registers)

Address-Computation Examples

%rdx	0xf000
%rcx	0x0100

Expression	Address Computation	Address
0x8(%rdx)	0xf000 + 0x8	0xf008
(%rdx, %rcx)	0xf000 + 0x100	0xf100
(%rdx, %rcx, 4)	0xf000 + 4*0x0100	0xf400
0x80(,%rdx, 2)	2*0xf000 + 0x80	0x1e080

Address-Computation Instruction

- leaq src, dest
 - src is address mode expression
 - set dest to address denoted by expression

• Uses

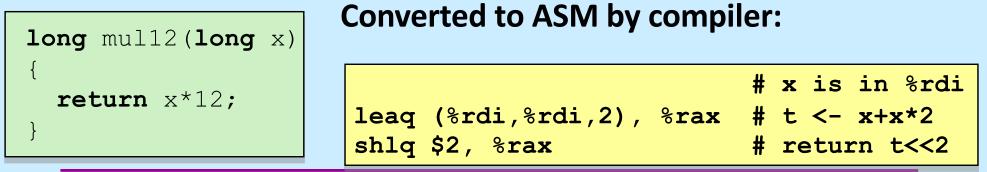
computing addresses without a memory reference

» e.g., translation of p = &x[i];

computing arithmetic expressions of the form x + k*y

» k = 1, 2, 4, or 8

• Example



32-bit Operands on x86-64

- addl 4(%rdx), %eax
 - memory address must be 64 bits
 - operands (in this case) are 32-bit
 - » result goes into %eax
 - lower half of %rax
 - upper half is filled with zeroes

Quiz 3

100	09: 0x09
What value ends up in %ecx?	08: 0x08
100 100 100 100 100 100 100 100 100 100	07: 0x07
	06: 0x06
	05: 0x05
	04: 0x04
movl 2(%rax,%rbx,2),%ecx 100	03: 0x03
a) 0x04050607 100	02: 0x02
	01: 0x01
c) $0x06070809$ %rax $\rightarrow 100$	00: 0x00
d) 0x09080706	
Hint:	

X–33

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